CLAIMS

What is claimed is:

1. A microelectronic device, comprising:

a microelectronic die having an active surface, a back surface, and at least one side;

said at least one microelectronic die side comprising at least one trench sidewall, at least one lip and at least one channel sidewall; and

a metallization layer disposed on said microelectronic die back surface and said at least one trench sidewall.

2. The microelectronic device of claim 1, wherein said at least one trench sidewall is substantially planar to said at least one channel sidewall.

3. The microelectronic device of claim 2, wherein said at least one lip is substantially perpendicular to at least one of said at least one trench sidewall and at least one channel sidewall.

4. The microelectronic device of claim 2, wherein said at least one lip is substantially angled to at least one of said at least one trench sidewall and at least one channel sidewall.

5. The microelectronic device of claim 2, wherein said at least one lip is substantially curved to at least one of said at least one trench sidewall and at least one channel sidewall.

6. The microelectronic device of claim 1, wherein said metallization layer is at least one metal selected from the group consisting of gold, silver, titanium, chromium, vanadium, tungsten, and nickel.

7. A microelectronic device assembly, comprising:

a microelectronic die having an active surface, a back surface, and at least one side;

said at least one microelectronic die side comprising at least one trench sidewall, at least one lip, and at least one channel sidewall;

a metallization layer disposed on said microelectronic die back surface and said at least one trench sidewall; and

a heat dissipation device attached to said microelectronic die back surface with a thermal interface material.

8. The microelectronic device assembly of claim 7, wherein said at least one trench sidewall is substantially planar to said at least one channel sidewall.

9. The microelectronic device assembly of claim 8, wherein said at least one lip is substantially perpendicular to at least one of said at least one trench sidewall and at least one channel sidewall.

10. The microelectronic device of claim 8, wherein said at least one lip is substantially angled to at least one of said at least one trench sidewall and at least one channel sidewall.

11. The microelectronic device of claim 8, wherein said at least one lip is substantially curved to at least one of said at least one trench sidewall and at least one channel sidewall.

12. The microelectronic device assembly of claim 7, wherein said metallization layer is at least one metal selected from the group consisting of gold, silver, titanium, chromium, vanadium, tungsten, and nickel.

13. The microelectronic device assembly of claim 7, wherein said thermal interface material is selected from the group consisting of lead, tin, indium, silver, copper, and alloys thereof.

14. The microelectronic device assembly of claim 7, wherein at least a portion of a fillet of said thermal interface material extend from said metallization layer on said microelectronic die trench sidewall to said heat dissipation device.

15. A method of dicing a microelectronic device wafer, comprising:

providing a microelectronic device wafer comprising a semiconductor wafer having a back surface, said microelectronic device including at least two integrated circuit areas formed therein separated by at least one scribe street;

forming at least one trench opposing said at least one scribe street and extending from said semiconductor wafer back surface into said semiconductor wafer, wherein said trench comprises at least two sidewalls and a bottom portion;

forming a metallization layer on said semiconductor wafer back surface, said at least two trench sidewalls and said trench bottom portion; and

forming a channel within said at least one scribe street and extending through said interconnection layer, said semiconductor wafer, and said metallization layer in said trench bottom portion.

16. The method of claim 15, wherein providing said microelectronic further includes providing said microelectronic device wafer having an interconnection layer disposed on said active surface.

17. The method of claim 15, wherein forming said trench comprises forming at least one trench that is wider than said channel.

18. The method of claim 15, wherein forming said trench comprises forming said trench by a method selected from the group consisting of laser ablation, wet etching, dry etching, reactive ion etching, and cutting with a wafer saw.

19. The method of claim 15, wherein forming said metallization layer comprises depositing a layer of metal selected from the group consisting of gold, silver, titanium, chromium, vanadium, tungsten, and nickel.

20. A method of fabricating a microelectronic device assembly, comprising:

providing a microelectronic die having an active surface, a back surface, and at least one side, wherein said at least one microelectronic die side comprises at least one trench sidewall, at least one lip and at least one channel sidewall;

disposing a metallization layer on said microelectronic die back surface and said at least one trench sidewall; and

attaching a heat dissipation device to said microelectronic die back surface with a thermal interface material.

21. The method of claim 20, wherein disposing said metallization layer comprises disposing a metal selected from the group consisting of gold, silver, titanium, chromium, vanadium, tungsten, and nickel on said microelectronic die back surface.

22. The method of claim 20, wherein attaching said heat dissipation device comprises attaching said heat dissipation device with a thermal interface material selected from the group consisting of lead, tin, indium, silver, copper, and alloys thereof.

23. The method of claim 20, wherein attaching said heat dissipation device comprises attaching said heat dissipation device with said thermal interface material such that a portion of a fillet of said thermal interface material extends from said metallization layer on said trench sidewall to said heat dissipation device.

24. The method of claim 20, wherein providing said microelectronic die comprises:

providing a microelectronic device wafer comprising a semiconductor wafer having a back surface, said microelectronic device including at least two integrated circuit areas formed therein separated by at least one scribe street;

forming at least one trench opposing said at least one scribe street and extending from said semiconductor wafer back surface into said semiconductor wafer, wherein said trench comprises at least two sidewalls and a bottom portion;

forming a metallization layer on said semiconductor wafer back surface, said at least two trench sidewalls and said trench bottom portion; and

forming a channel within said at least one scribe street and extending through said interconnection layer, said semiconductor wafer, and said metallization layer in said trench bottom portion.

25. The method of claim 24, wherein providing said microelectronic die further includes providing said microelectronic device wafer having an interconnection layer disposed on said active surface.

26. The method of claim 24, wherein forming said trench comprising forming at least one trench which is wider than said channel.

27. The method of claim 24, wherein forming said trench comprises forming said trench by a method selected from the group consisting of laser ablation, wet etching, dry etching, reactive ion etching, and cutting with a wafer saw.

28. The method of claim 24, wherein forming said metallization layer comprises depositing a layer of metal selected from the group consisting of gold, silver, titanium, chromium, vanadium, tungsten, and nickel.